F-02 ED0591

Dry Etching Method for Semiconductor Device

Background of the Invention

Field of the Invention:

The present invention relates to a dry etching method suitable for use in a semiconductor device, and particularly to a dry etching method suitable for use in a semiconductor device in which an N type polysilicon gate and a P type polysilicon gate exist in mixed form.

Description of the Related Art:

The scale-down or miniaturization of a semiconductor element has definitely been put forward at the request of the speeding up of an LSI and a reduction in its power consumption. As to a process for manufacturing a gate electrode in particular, the accuracy of its formation leads to the performance of a transistor, by extension, it is significantly related to the capability of the whole LSI. Therefore, this encounters a confrontation with a strict demand in particular. Simultaneously with an improvement in dimensional accuracy, there has also been a demand for an improvement in driving force of the transistor. In a prior device, the doping of a gate with an impurity has generally been performed on a self-alignment basis upon a source/drain ion implanting process after the patterning formation of the gate.

In this case, only a non-doped polysilicon (Poly-

Si) electrode may be etched in a gate patterning process. Since, however, this method is not capable of sufficiently obtaining the driving force of the transistor, a system (hereinafter called "dual gate system") for doping a gate electrode with an impurity in advance before etching now starts to be adopted. This system will cause a need to take into consideration the type of impurity and a difference in dimension due to impurity density in addition to a difference in dimension due to the loose/dense difference between patterns upon etching.

Fig. 1 shows the result of measurement of dimensions where the dual gate system is adopted. When etching conditions are set such that the dimension of an N type polysilicon gate is controlled constant, the dimension of a P type polysilicon gate greatly changes. When the amount of ion-implantation of an impurity is small, there is little difference in dimension, whereas when phosphor (P) and boron (B) are respectively ion-implanted into the gates by a dose of $5E15cm^{-2}$, a dimensional difference of about 0.037μm takes place. That is, it is understood that the difference in dimension between two types of different gate regions extends in proportion to a density difference.

When normal two-stage dry etching constituted of, for example, a main step (HBr/O_2 flow rate = 100/3 sccm, high-frequency power/low-frequency power = 250W/30W,

pressure: 1Pa and temperature: 60°C) and an overetching step (HBr/O_2/He flow rate = 100/2/100 sccm, high-frequency power/low frequency power = 250W/50W, pressure: 8Pa and temperature: 60°C) is performed, end point detection in the main step occurs in an N type polysilicon gate region fast in etching rate. Upon the end point detection, polysilicon in a P type polysilicon gate region still remains. Further, the remaining polysilicon is etched under an overetch condition corresponding to the next overetching step. Therefore, each P type polysilicon gate is assumed to be taper-shaped as shown in Fig. 2. This tendency takes place regardless of the looseness/denseness of patterns.

On the other hand, the technique of flattening an interlayer insulating film by chemical mechanical polishing or the like to ensure a margin by photolithography under a strict design rule with the scale-down of an LSI has been applied to a large number of devices. However, it is understood that since, however, the pressure at each point on a wafer changes because the pattern density is ununiform, the dependence of the pattern density on the amount of polishing occurs in the case of polishing. As a measure taken to cope with such a situation, there has been introduced such a contrivance that dummy patterns are fabricated to reduce the difference in density between the patterns in the wafer.

A polysilicon layer has been used for many kinds of

elements such as resistance wiring, a capacitor electrode, etc. as well as a gate electrode of a transistor. The type and density of impurity to be introduced also come in many forms and correspondingly, ion-implantation conditions also vary widely. Depending on the devices, there have been considered various forms such as a case in which a region subjected to ion implantation and a region with no ion implantation exist in mixed form on the same wafer, the use of a non-doped polysilicon gate perfectly unsubjected to ion implantation, etc.

Patent documents 1 through 3:

Japanese Unexamined Patent Publication No. 2000-58511

Japanese Unexamined Patent Publication No. 2000-164732

Japanese Unexamined Patent Publication No. Hei 11(1999)-204506

As described above, the dual gate type device has a problem in that when the N type polysilicon gate and the P type polysilicon gate are simultaneously dry-etched, it is difficult to control them to the same finished dimension. As a result, a problem has arisen that the miniaturization of the transistor and an improvement in the performance thereof have been impaired.

Summary of the Invention

The present invention has been made in view of the above problems. The present invention aims to provide a semiconductor device comprising an N type polysilicon gate and a P type polysilicon gate both disposed

simultaneously, wherein a dummy gate made of non-doped polysilicon is disposed for polysilicon gate etching and set so as to take an area larger than the total area of the N type polysilicon gate and the P type polysilicon gate, followed by patterning of polysilicon gate electrodes.

The present invention provides a device in which both an N type polysilicon gate and a P type polysilicon gate are disposed in mixed form, wherein the area of a non-doped polysilicon gate corresponding to a dummy electrode is set larger than the total area of the N type and P type doped polysilicon gates, thereby to make it possible to control etching of the polysilicon gates so as to be rate-controlled in a non-doped region and to reduce the difference in etching dimension between the N type polysilicon gate and the P type polysilicon gate. As a result, the miniaturization of the device having the N type and P type polysilicon gates and an improvement in its performance are enabled and hence an LSI high in reliability can be realized.

Brief Description of the Drawings

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and

advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a view showing problems on dry etching of gate electrodes employed in a prior art;

Fig. 2 is a view illustrating dry-etched shapes of the gate electrodes employed in the prior art; and

Fig. 3 is a dry etching process sectional view for describing an embodiment of the present invention.

Detailed Description of the Invention

A first embodiment of the present invention will be explained. Although not shown in the drawing, a gate insulating film is formed on a silicon substrate 1 and thereafter a polysilicon layer 2 constituted as gate electrodes is deposited thereon. Next, a resist 3 is subjected to patterning. Phosphor (P) ions are selectively implanted into a region 4 for forming an N type channel transistor gate (see Fig. 3(a)). Boron (B) ions are selectively implanted into a region 5 for forming a P type channel transistor gate (see Fig. 3(b)). At this time, no impurity is injected into a dummy gate electrode region 6. Subsequently, patterning is done by a lithography technique and the non-doped polysilicon and doped polysilicon regions 4 and 5 in the dummy gate electrode region 6 are etched to form gate electrodes (see Fig. 3(c)).

When, for example, chemical mechanical polishing is performed, dummy patterns are disposed to reduce variations in the polishing amount. However, when dummy gate patterns are disposed on a mask, the proportion of the dummy gate patterns made of non-doped polysilicon is set so as to become larger than the proportion of dummy gate patterns made of doped polysilicon. As a result, the end point detection of gate electrode etching in a main step at the gate electrode etching is rate-controlled by etching of the non-doped polysilicon. Thus, the etching rate at the gate electrode etching can be set so as to be substantially determined by the corresponding dummy gate corresponding to the non-doped polysilicon.

After a polysilicon layer has been ion-implanted over its entire surface, the polysilicon layer was etched under etching conditions similar to the prior art and its etching rate was measured. When P ions are implanted $5E15cm^{-2}$, the end point detection of etching of polysilicon is carried out in 35 seconds, whereas when B ions are implanted $5E15cm^{-2}$, the end point detection under the same etching conditions needs a time interval of 55 seconds. It is understood that the end point detection is done in 45 seconds in the case of the non-doped polysilicon free of ion implantation, and the etching rate greatly changes with the ion implantation.

This is because such a phenomenon occurs due to the fact that the etching of the polysilicon layer in the P

type polysilicon gate region is not yet ended at the detection of the etching end point in the N type polysilicon gate region, and the polysilicon layer that remains in high-pressure overetching corresponding to the next step is etched so that each resultant polysilicon layer in the P type region is taper-shaped as shown in Fig. 2. Therefore, the end point detection time is prolonged up to the time determined according to the etching rate in the non-doped polysilicon region, thereby making it possible to reduce the amount of taper in the P type region and hence reduce a difference in dimension due to ion species.

Incidentally, although excessive etching is applied to the polysilicon layer in the N type region upon overetching for reducing the amount of taper in the P type region, a product yielded by reaction with HBr gas used in etching is deposited on each polysilicon gate sidewall. Therefore, side etching in a transverse direction does not make progress and hence a change in gate dimension in the N type region at overetching is less reduced.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art

on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention..